UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,845	07/10/2003	Sterling Smith	MSS-0003-US	9986

36183 7590 06/12/2007

PAUL, HASTINGS, JANOFSKY & WALKER LLP
P.O. BOX 919092
SAN DIEGO, CA 92191-9092

EXAMINER	
VLAHOS, SOPHIA	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
06/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/615,845	SMITH, STERLING	
	Examiner	Art Unit	
	SOPHIA VLAHOS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6 and 15* is/are allowed.

6)☒ Claim(s) *1-5 and 7-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 7-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Riley (U.S. 4,965,531) in view Mathe et. al. (U.S. 5,825,253).

With respect to claim 1, Riley discloses: a divider for receiving a reference clock with a substantially fixed period and generating an output clock with a time-varying period (see Fig. 4, where the reference frequency fr corresponds to the reference clock with substantially fixed period and fod corresponds to the clock with a time-varying period since the divider 106 is controlled by time varying signal b(t) out of the sigma-delta modulator 102, and the output clock has time varying frequency (period) since fr is divided by n , n+1 (see column 4,lines 66-67,column 5, lines 1-2 describing similar functions of the system shown in Fig. 2); a noise-shaped quantizer for quantizing a period control word to a time-varying value in response to said output clock fed from said divider so that said divider generates said output clock by means of dividing said reference clock by said time-varying value (see sigma-delta modulator 102 which is a noise-shaped quantizer since b(t) that includes quantization noise is fed-back to control mux 206 (where quantization noise is inherent in b(t) see column 5, lines 38-40), the period control words is signal 212 which corresponds to $\delta\Phi$ plus/minus Ref (see Fig.

4)(see column 3, lines 22 and column 4, lines 48, since δΦ is the frequency (period) control signal signal 212 is a frequency (period) control word plus/minus REf) time varying signal b(t) shown in Fig, 4 (and the corresponding parts of Fig. 2) and see column 5, lines 38-40, where b(t) is a quantized 1-bit signal); means for adjusting said period control word by a period offset in response to said output clock, wherein said period control word is within a period range with reference to a period nominal (the claimed means corresponds to mux 204 and blocks 208, 210 that are part of the sigma-delta modulator, see Fig. 2 where b(t) s fed-back to mux 206 and selects "+Ref" or "–Ref" (the frequency (period) offset) supplied to adder 202, and see that the "period control word" 212 is adjusted by the plus/minus Ref value, and the (frequency) period control word is δΦ plus/minus Ref, i.e. within a frequency (period) range with reference to a frequency (period) nominal δΦ

Riley does not expressly teach: a filter for substantially filtering out jitter from said output clock.

In the same field of endeavor Mathe et. al., disclose: a filter for substantially filtering out jitter from output clock (see Fig. 2, PLL comprising elements 106, 108, 110, 112 filtering the "event clock", see column 4, lines 35-67, column 5, line 1).

At the time of the invention, it would have been obvious to a person skilled in the art to modify the system of Riley so that it includes a filter for substantially filtering out jitter from output clock (as taught by Mathe et. al.,) and the motivation for incorporating the filter of Riley in the system of Riely would be to obtain good phase noise characteristics in the clock signal (see column 4, lines 51-52 of Mathe et. al.,).

With respect to claim 2, Riley discloses: wherein said period control word has a bit resolution greater than that of said time-varying value (column 5, lines 38-40, where the output of the sigma-delta modulator, ie. b(t) has 1-bit resolution, whereas signal 212 is the addition of the multiple bit signal $\delta\Phi$ and +-Ref see column 5, lines 20-29).

With respect to claim 3, Riley discloses: wherein said noise-shaped quantizer is a delta-sigma quantizer (Fig. 4, block 102, delta-sigma modulator that performs quantization).

With respect to claim 4, all of the limitations of claim 4 are rejected above in claim 1.

With respect to claim 5, Riley discloses: wherein said means for adjusting said period control word comprises: an offset generator for generating said period offset in response to said output clock (see mux 204 that "generates" the offset when it selects the :+Ref" or "-Ref", and blocks 208, 210 that are part of the sigma-delta modulator, see Fig. 2 and b(t) controls the mux therefore the period offset is generated in response to fd (fod output clock for Fig. 4) since b(t) is generated in response to fd (see elements 214, 215, 218 that generate b(t) are clocked (function in response to fd) with fd) ; and an adder for generating said adjusted period control word by means of adding said period offset to said a period nominal (see Fig. 2, adder 202).

Claims 7-14 are rejected under a similar rationale used to reject claims 1-5 above. Specifically claims 7-8 and 10-11 are rejected similarly to claim 1 above. Claims 9, 12, 13, 14 are rejected similarly to claims 4, 2, 3, 5 respectively.

Allowable Subject Matter

3. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of the record fails to teach or suggest alone or in combination: A digital spread spectrum frequency synthesizer, comprising: means for adjusting said period control word comprises: an offset generator for generating said period offset in response to said output clock; and an adder for generating said adjusted period control word by means of adding said period offset to a period nominal, wherein said offset generator s an up/down counter, as recited in claim 6 and in combination with other elements of the claim.

Claim 6 is allowed.

The prior art of the record fails to teach or suggest alone or in combination: A digital spread spectrum frequency synthesizer, comprising: means for adjusting said period control word by a period offset in response to said output signal, wherein said means for adjusting said period control word, comprises: an offset generator for generating for

generating said period offset in response to said output clock; and an adder for generating said adjusted period control word by means of adding said period offset to a period nominal, wherein said offset generator is an up/down counter, as recited in claim 15 and in combination with other elements of the claim.

Claim 15 is allowed.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SOPHIA VLAHOS whose telephone number is 571 272 5507. The examiner can normally be reached on MTWRF 8:30-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SV
5/30/2007

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER